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U.S. Patent and Trademark Office; U.S. DEPARTMENT OF COMMERCE



| PRE-APPEAL BRIEF REQUEST FOR REVIEW | Docket Number (Optional) SON-3058 | |
|---|---|---|
| | Application Number 10/564,473-Conf. #9263 | Filed January 13, 2006 |
| | First Named Inventor Masaki Murase | |
| | Art Unit 2629 | Examiner G. Sitta |

Applicant requests review of the final rejection in the above-identified application. No amendments are being filed with this request.

This request is being filed with a notice of appeal.

The review is requested for the reason(s) stated on the attached sheet(s).
Note: No more than five (5) pages may be provided.

I am the

- [ ] applicant /inventor.
- [ ] assignee of record of the entire interest. See 37 CFR 3.71. Statement under 37 CFR 3.73(b) is enclosed. (Form PTO/SB/96)
- [x] attorney or agent of record. Registration number 40,290/47,255
- [ ] attorney or agent acting under 37 CFR 1.34. Registration number if acting under 37 CFR 1.34. _____

Signature

Christopher M. Tobin/Brian K. Dutton
Typed or printed name

(202) 955-3750
Telephone number

November 19, 2009
Date

NOTE: Signatures of all the inventors or assignees of record of the entire interest or their representative(s) are required. Submit multiple forms if more than one signature is required, see below*.

[x] *Total of 1 forms are submitted.

Docket No.: SON-3058
(PATENT)

**IN THE UNITED STATES PATENT AND TRADEMARK OFFICE**

In re Patent Application of:
Masaki Murase et al.

Application No.: 10/564,473 | Confirmation No.: 9263

Filed: January 13, 2006 | Art Unit: 2629

For: DELAY TIME CORRECTION CIRCUIT, VIDEO DATA PROCESSING CIRCUIT, AND FLAT DISPLAY DEVICE | Examiner: G. Sitta

**REQUEST FOR PRE-APPEAL BRIEF PANEL REVIEW OF REJECTION**

MS AF
Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

Dear Sir:

This is in full and timely response to the Office Communication dated August 20, 2009.

Claims 7-22 are currently pending in this application, with claim 7 being independent.

1. **Claims 7-22** - Claims 8-22 are dependent upon claim 7. Claim 7 is drawn to a display device comprising:

> a level shifter configured to change an amplitude of gradation data from a first voltage range to a second voltage range, amplified gradation data being said gradation data at said second voltage range,
>
> wherein output data during a quiescent period is dummy data, said output data during a period other than said quiescent period being said amplified gradation data.

2. **"Background Art" of the specification for the present application (AAPA)** – The Office Action contends that AAPA discloses the presence of a level shifter (fig. 1 (1)) (Office Action at page 2).

However, the Office Action ***readily admits*** that AAPA ***fails*** to teach wherein output data during a quiescent period is dummy data (Office Action at page 3).

- ***Thus, AAPA fails to disclose, teach, or suggest a display device wherein output data during a quiescent period is dummy data, said output data during a period other than said quiescent period being said amplified gradation data.***

3. **Japanese Application Publication No. 2002-009594 (Iemoto)** – The Office Action cites Iemoto for the features that are admittedly absent from within Iemoto.

In response, the machine translation of Iemoto arguably discloses the following at paragraph [0010]:

> [0010]Although *the **vernier 10** is a circuit which acquires a time delay with the variable resolution below a reference signal*, since it has a time delay more than the cycle of a reference signal at least including the fixed delay of a vernier at the time of maximum delay setting out, compared with other logic gates, the delay time variations to a temperature change will become large.

The machine translation of Iemoto arguably discloses the following at paragraphs [0024]-[0026]:

> [0024]The delay circuit 32 is larger than the time delay of the flip-flop 20, and delays the inputted reference signal RCLK within the time of the cycle T and the difference of pulse width of the reference signal RCLK, and *outputs **delay clock signal DCLK** to OR gate 50 **as a dummy pulse signal***.

[0025]OR gate 50 carries out OR operation of the ***delay clock signal DCLK*** inputted as signal TM2 inputted from the flip-flop 20 from the delay circuit 32, and outputs it to the vernier 10 as ***mix-signals TD3***.

[0026]*The vernier 10 delays* ***mix-signals TD3*** inputted from OR gate 50 according to a preset value by the time resolution below the cycle T of the reference signal RCLK, and *outputs it* to the delay circuit 42 and the flip-flop 41 as *delay pulse signal TD4*.

However, Iemoto ***fails*** to disclose, teach, or suggest ***mix-signals TD3*** as including amplified gradation data.

- ***Thus, Iemoto fails to disclose, teach, or suggest a display device wherein output data during a quiescent period is dummy data, said output data during a period other than said quiescent period being said amplified gradation data.***

4. **Combination of AAPA and Iemoto as a whole** – The Office Action contends that it would have been obvious to one of ordinary skill in the art, at the time of the invention, to incorporate the dummy data during a quiescent period as taught by Iemoto in order to reduce fluctuations in the operating frequency of the circuit as stated in the abstract of Iemoto (Office Action at page 3).

**Figure 1 of Iemoto**

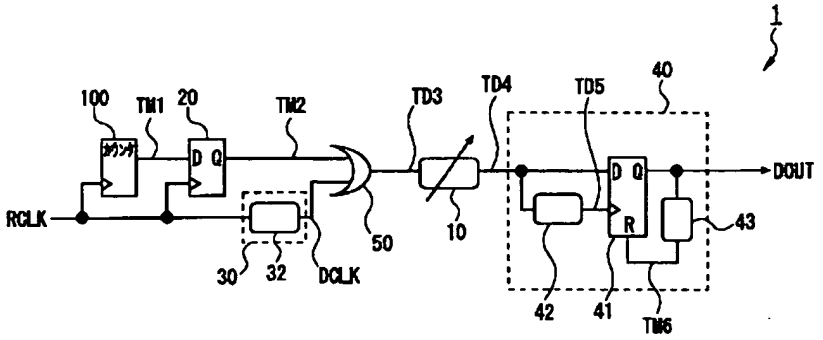



**Figure 1 of AAPA**

A review of Iemoto reveals an ***absence*** of a level shifter within Figure 1 of Iemoto.

The Office Action ***fails*** to show where, how and why the level shifter 1 of AAPA would have been integrated into the circuitry of Iemoto.

The Office Action ***fails*** to show the alleged output data of AAPA and the alleged output data of Iemoto as being one in the same.

**Figure 2 of Iemoto**

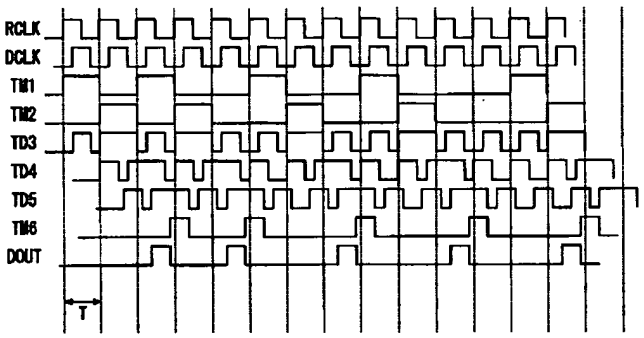
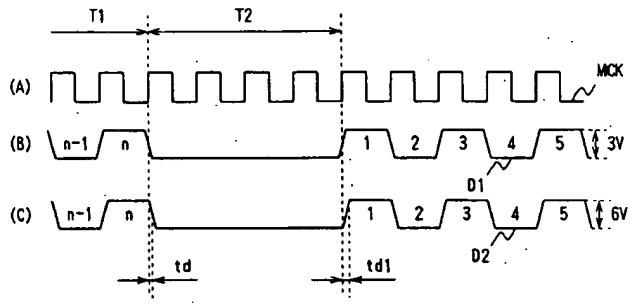



**Figure 2 of AAPA**




Regarding AAPA, paragraph [0009] of U.S. Patent Application Publication No. 2006/0164364, the priority document for the present application, provides the presence of a ***period T2***.

However, Iemoto reveals an ***absence*** of a ***time period T2*** within Iemoto.

Moreover, the Office Action ***fails*** to show the time periods for the alleged quiescent period of AAPA and the alleged quiescent period of Iemoto as being one in the same.

The Office Action attempts an association of the delay clock signal DCLK of Iemoto with the claimed dummy data (Office Action at page 3).

Likewise, the Office Action apparently attempts an association of the output data D2 of AAPA with the claimed amplified gradation data (Office Action at page 2).

However, the Office Action ***fails*** to show how and why the skilled artisan would have considered any of the mix-signals TD3 of Iemoto as including ***amplified*** gradation data.

The Office Action ***fails*** to show where and how the output data would have been gradation data from AAPA in one instance and any of the mix-signals TD3 from Iemoto in the next instance, especially when there is no disclosure of time T2 of AAPA within Iemoto.

5. **U.S. Patent No. 6,897,909 (Ochiai)** – Ochiai arguably discloses that the term "polysilicon" also encompasses macrocrystalline silicon and ***continuous grain silicon (CGS)*** as well as single-crystal silicon (Ochiai at column 23, lines 48-50).

- ***However, Ochiai fails to disclose, teach, or suggest a display device wherein output data during a quiescent period is dummy data, said output data during a period other than said quiescent period being said amplified gradation data.***

**Conclusion**

If the Examiner has any comments or suggestions that could place this application in even better form, the Examiner is requested to telephone Brian K. Dutton, Reg. No. 47,255, at 202-955-8753.

Dated: November 19, 2009

Respectfully submitted,

By_____
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